IN THE CLAIMS

1. (Currently Amended) A subthreshold current-efficient buffer comprising:

first and second inverters connected in series;

a memory cell;

an NMOS transistor controlled by the memory cell and connected between the second inverter and ground; and

a PMOS transistor controlled by a complemented output of the memory cell and connected between the first inverter and a power source.

2. (Cancelled)

3. (Original) The subthreshold current-efficient buffer of claim 1 where the first inverter comprises a PMOS transistor manufactured to sit in a voltage well biased with a higher voltage than that of a power supply.

4. (Currently Amended) A subthreshold current-efficient circuit comprising:

first and second buffers, each buffer having two inverters connected in series;

an NMOS transistor connected in series between ground and the second inverter of each buffer; and

a PMOS transistor connected in series between a power source and the first inverter of each buffer.

5. (Currently Amended) The subthreshold current-efficient circuit of claim 4 further comprising a memory cell controlling both the NMOS transistor and the PMOS transistor.

6. (Original) The subthreshold current-efficient circuit of claim 4 wherein the first and second buffers each comprise PMOS transistors manufactured to sit in a voltage well biased with a higher voltage than that of a power supply.

7. (Currently Amended) The subthreshold current-efficient circuit of claim 6 wherein the PMOS transistors in the first and second buffers form part of the first inverter of each buffer.

8. (Currently Amended) In a field programmable device having logic blocks and a routing matrix, an improved subthreshold current-efficient circuit comprising:

at least one buffer for driving signals onto a signal line of the routing matrix;

an NMOS transistor connected between ground and the at least one buffer;

a PMOS transistor connected between power and the at least one buffer; and

a memory cell connected to control the NMOS transistor and the PMOS transistor and turn ~~it~~ them off when the at least one buffer is unused.

9. (Cancelled)

10. (Original) The field programmable device of claim 8 wherein the buffer comprises at least one PMOS transistor manufactured to sit in a voltage well biased with a higher voltage than that of a power supply.

11. (Currently Amended) In a field programmable device having CLEs and a routing matrix, an improved subthreshold current efficient circuit comprising:

a plurality of buffers for driving signals on signal lines of the routing matrix, the plurality of buffers being grouped in pairs wherein each buffer pair comprises an NMOS transistor connected between ground and the buffer pair and a PMOS transistor connected between a power source and the buffer pair;

a corresponding memory cell connected to control each NMOS and PMOS transistor and turn ~~it~~ them off when ~~its~~ their associated buffer pair is unused.

12. (Cancelled)

13. (Original) The field programmable device of claim 11 wherein the plurality of buffers comprise at least one PMOS transistor manufactured to sit in a voltage well biased with a higher voltage than that of a power supply.

14. (Currently Amended) A method of reducing subthreshold current in a field programmable device (FPD) comprising the steps of:

providing virtual ground transistors on selected buffers within an FPD;

providing virtual power transistors on the selected buffers;

providing memory cells to control the state of the virtual ground and power transistors;

programming the memory cells to turn off the virtual ground and power transistors of the buffers that are not being used.

15. (Cancelled)

16. (Original) The method of claim 14 further comprising providing selected buffers within the FPD which have PMOS transistors manufactured to sit in a voltage well biased with a higher voltage than that of a power supply.

17. (Currently Amended) The method of claim 14 further comprising providing virtual ground and power transistors to control logic gates used as the first stage of a buffer.

REMARKS

No new matter has been introduced by any of the above amendments. In light of the above amendments and remarks, Applicant believes that Claims 1, 3-8, 10-11, 13-14, and 16-17 are in condition for allowance, and allowance of the application is therefore requested. If any action other than allowance is contemplated by the Examiner, the Examiner is respectfully requested to telephone Applicant's agent, Lois D. Cartier, at 720-652-3733.

Respectfully submitted,

Lois D. Cartier
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I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, on August 12, 2003.

Pat Slaback
Name

Signature